Fully Integrated Overcurrent Protection Method During SiC MOSFET Conduction

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***Abstract*—A gate driver IC with fully integrated overcurrent protection functions developed for IGBTs is successfully applied to overcurrent protection for SiC MOSFETs. In the gate driver IC, while the SiC MOSFETs are ON, constant gate charge is periodically discharged and charged, and when gate-to-source voltage dropped by each discharge is less than the reference voltage, it is detected as the overcurrent and the SiC MOSFETs are immediately turned off to protect from the overcurrent. Overcurrent protection can be achieved at low cost, since external components such as high-voltage diodes are not required. While the overcurrent detection threshold is constant and cannot be changed for IGBTs, it is found for the first time in SiC MOSFETs that the overcurrent detection threshold can be varied by changing the gate charge to be discharged. In a single-pulse test of an inductive load at 300 V for an SiC MOSFET with DC rating of 134 A and pulse rating of 240 A, the gate driver IC successfully protected the overcurrent with the protection delay of 226 ns or less, while the overcurrent detection threshold is variable in the range of 104 A to 306 A.**

Keywords— overcurrent, protection, gate driver, IC, gate voltage, SiC

I. Introduction

Overcurrent detection and protection of power devices are important technologies to realize reliable power electronic systems. The target of this work is to develop an overcurrent protection method for SiC MOSFETs used in large-current, short-pulse current generator circuits with an inductive load [1] that (1) can be fully integrated into a gate driver IC without external components such as high-voltage diodes for low cost, (2) can detect overcurrent while the SiC MOSFETs are ON, and (3) has a variable overcurrent detection threshold (I_{TH}).

Table I shows a summary of conventional detection and protection for overcurrent. Methods for detecting overcurrent by measuring drain current (I_D) [2-5], and drain-to-source voltage (V_{DS}) [3, 6] of SiC MOSFETs have been proposed. I_D measurement requires a current sensor, and V_{DS} measurement for desaturation detection requires a high-voltage diode, which are expensive. All conventional overcurrent detection methods by gate-to-emitter voltage (V_{GE}) measurement in IGBTs [7, 8, 10] and gate-to-source voltage (V_{GS}) measurement in SiC MOSFETs [9, 11] have the disadvantage that overcurrent during ON of IGBTs/SiC MOSFETs cannot be detected, because V_{GE}/V_{GS} is measured during the turn-on transient. No conventional overcurrent protection methods, however, satisfy all three targets.

TABLE I. Comparison Table of Detection and Protection For Overcurrent

Reference	[2-5]	[3, 6]	[10]	[11]	[12]	This work
Method	Current monitor	Desaturation	V_{GE} at Miller plateau	Gate charge	MGDC	MGDC
Measured value	I_D	V_{DS}	V_{GE}	Q_G, V_{GS}	V_{GE}	V_{GS}
Power device	SiC	SiC	IGBT	SiC	IGBT	SiC
Measurement from gate terminal	No	No	Yes	Yes	Yes	Yes
Overcurrent detection during ON	Yes	Yes	No	No	Yes	Yes
Fully integrated protection	No	No	No	No (Only detection)	Yes	Yes
Variable threshold for overcurrent detection	Yes	Yes	Yes	No	No	Yes by VDOS
Detection / protection delay [ns]	22 [2] 100 [3]	250 [3] 400 [6]	500	369	810	< 226

Therefore, in this paper, an overcurrent protection method for SiC MOSFETs that satisfies all three targets is proposed by applying the gate driver IC [12] with a fully integrated overcurrent protection function called "monitoring gate voltage while periodically repeating discharging and charging of constant gate charge (MGDC) [13]" developed for IGBTs to SiC MOSFETs. When the gate driver IC [12] is applied to SiC MOSFETs, a new phenomenon called "V_{GS} drop due to overheating of SiC (VDOS)" is found. Therefore, the variable I_{TH} using the phenomenon is achieved in this paper.

II. Proposed Fully Integrated Overcurrent Protection

A. Gate Driver IC with Fully Integrated Overcurrent Protection

Fig. 1 shows an operation principle of the gate driver IC [12] with a fully integrated overcurrent protection function by measuring gate-to-source voltage (OPV) while SiC MOSFETs are ON. Two functions, a periodic constant gate charge (Q_C) discharger and recharger, and an overcurrent protection by V_{GS}, are added to the gate driver IC. While the SiC MOSFETs are ON, the periodic Q_C discharger and recharger periodically discharges and recharges Q_C. When V_{GS} dropped by each discharge is less than the reference voltage (V_{REF}), it is detected as the overcurrent

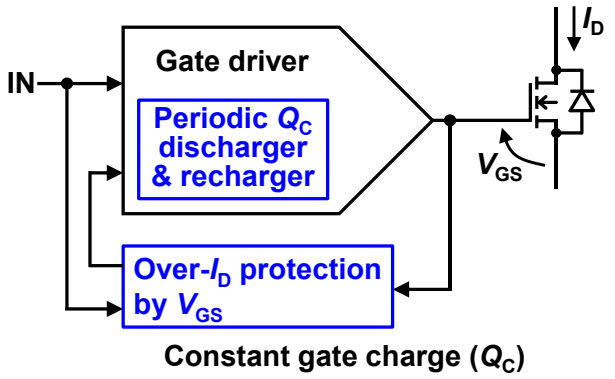

Fig. 1. Operation principle of gate driver IC with fully integrated overcurrent protection function by measuring V_{GS} (OPV).

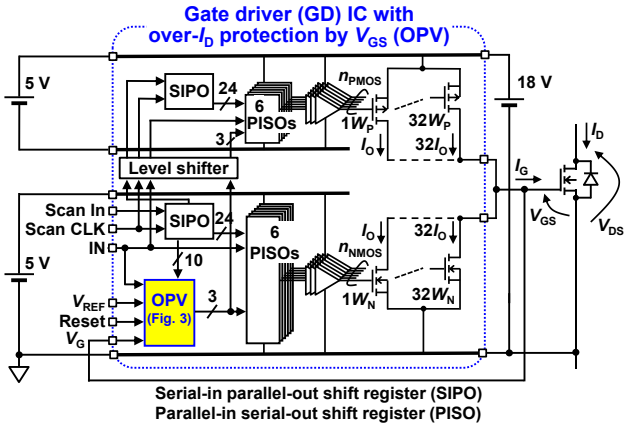

Fig. 2. Circuit schematics of gate driver IC with OPV.

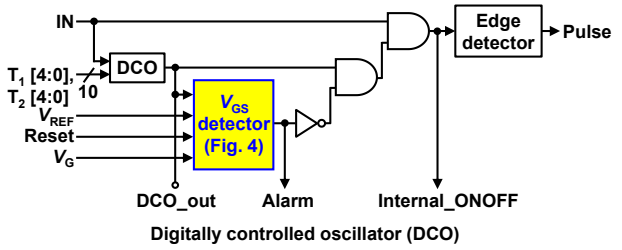

Fig. 3. Circuit schematics of OPV circuits.

and the gate driver is forced to turn off to complete the overcurrent protection.

Fig. 2 shows a circuit schematics of the gate driver IC with OPV [12]. All circuits are integrated on a single chip except for the isolated power supplies. To achieve the two functions shown in blue in Fig. 1, an OPV circuit is added to our previously developed 6-bit current-source type digital gate driver [14, 15] with variable gate current (I_G) in 64 levels, where $I_G = n_{PMOS} \times 40$ mA and n_{PMOS} is an integer from 0 to 63 at turn-on. At turn-off, $|I_G| = n_{NMOS} \times 41$ mA and n_{NMOS} is an integer from 0 to 63 at turn-on.

Fig. 3 shows a circuit schematics of the OPV circuits [12]. The OPV circuits include a digitally controlled oscillator (DCO) to determine charging and discharging time and a V_{GS} detector to detect the overcurrent by comparing V_{GS} and V_{REF}. The three

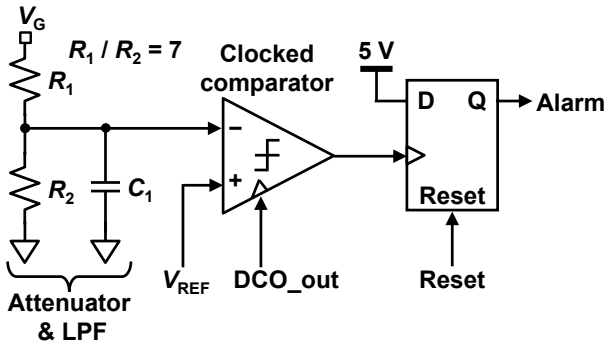

Fig. 4. Circuit schematics of V_{GS} detector.

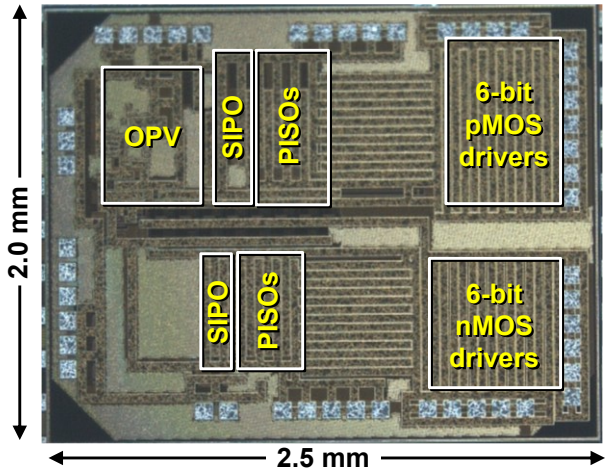

Fig. 5. Die photo of gate driver IC with OPV fabricated with 180-nm BCD process.

outputs of the OPV circuits (Alarm, Internal_ONOFF, and Pulse) are fed into the low-side and high-side parallel-in serial-out shift registers (PISOs) in Fig. 2.

Fig. 4 shows a circuit schematics of the V_{GS} detector [12]. The V_{GS} detector includes an attenuator with an attenuation ratio of one-eighth to prevent the input gate voltage (V_G) from damaging the clocked comparator with overvoltage, and a low pass filter (LPF) with a cutoff frequency of 57 MHz to remove high-frequency ringing of V_G. When the attenuated and low pass filtered V_G drops below V_{REF}, Alarm output changes from low to high, forcing the SiC MOSFET to turn off. Fig. 5 shows a die photo of the gate driver IC [12] with OPV fabricated with 180-nm BCD process. The die size is 2.0 mm by 2.5 mm.

B. Proposed Overcurrent Protection Using MGDC

Fig. 6 shows timing charts of the proposed overcurrent protection using MGDC. Table II shows the summary of the measured four parameters (t_1, t_2, I_1, and $|I_2|$) that can be digitally controlled by this IC to achieve MGDC [13]. The gate driver IC has a total of 22 control bits including T_1 [4:0], T_2 [4:0], I_1 [5:0], and I_2 [5:0]. All control bits are written in advance to the on-chip memory (two serial-in parallel-out shift registers (SIPOs) in Fig. 2) by scan-in, eliminating the need for the high-speed digital signal generator to determine t_1 and t_2.

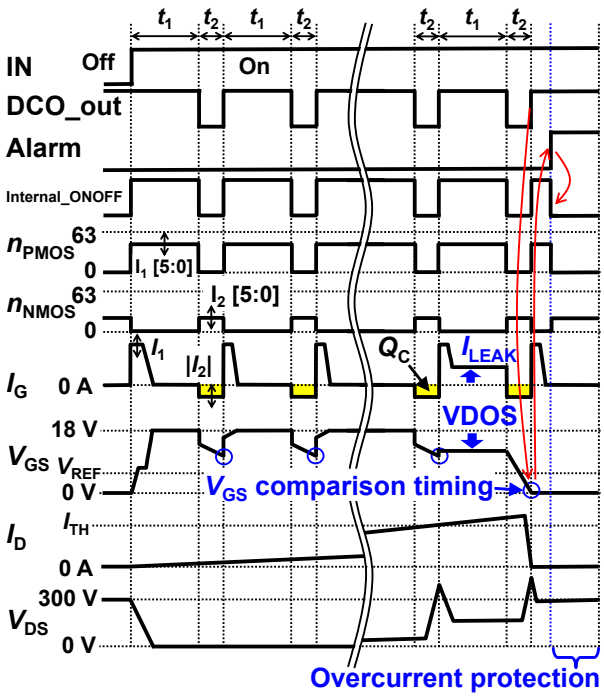

Fig. 6. Timing charts of proposed overcurrent protection using MGDC.

TABLE II. MEASURED FOUR PARAMETERS DIGITALLY CONTROLLED BY IC TO ACHIEVE MGDC

Parameters	Control bits	Range	Step
t_1	T_1 [4:0]	0 s to 17 µs	535 ns
t_2	T_2 [4:0]	0 s to 3.4 µs	110 ns
I_1	I_1 [5:0]	0 A to 2.5 A	40 mA
$\|I_2\|$	I_2 [5:0]	0 A to 2.6 A	41 mA

Figs. 7 to 10 show the measured t_1 vs. T_1 [4:0], t_2 vs. T_2 [4:0], I_1 vs. I_1 [5:0], and $|I_2|$ vs. I_2 [5:0], respectively. The charging time (t_1) of MGDC in Fig. 6 is digitally controlled by 5-bit T_1 [4:0] of DCO from 0 s to 17 µs in 535 ns steps as shown in Fig. 7. The charging gate current (I_1) during t_1 in Fig. 6 is digitally controlled by 6-bit I_1 [5:0] of the digital gate driver from 0 A to 2.5 A in 40 mA steps as shown in Fig. 9. Similarly, the discharging time (t_2) of MGDC in Fig. 6 is digitally controlled by 5-bit T_2 [4:0] of DCO from 0 s to 3.4 µs in 110 ns steps as shown in Fig. 8. The discharging gate current ($|I_2|$) during t_2 in Fig. 6 is digitally controlled by 6-bit I_2 [5:0] of the digital gate driver from 0 A to 2.6 A in 41 mA steps as shown in Fig. 10.

In MGDC in Fig. 6, while the SiC MOSFETs are ON, Q_C (= $|I_2| \times t_2$) is periodically discharged and recharged with the $t_1 + t_2$ cycle. $n_{PMOS} = I_1$ [5:0] and $n_{NMOS} = 0$ in the t_1 period, while $n_{PMOS} = 0$ and $n_{NMOS} = I_2$ [5:0] in the t_2 period. When V_{GS} dropped by each discharge is greater than V_{REF}, it is judged normal, and when V_{GS} dropped by each discharge is less than V_{REF}, it is detected as the overcurrent and the SiC MOSFETs are immediately turned off to protect from the overcurrent. V_{REF} should be set lower than V_{GS} after the first discharge and higher than V_{GS} when the overcurrent occurs. Unlike IGBTs, VDOS is found for the first time to occur in MGDC of SiC MOSFETs.

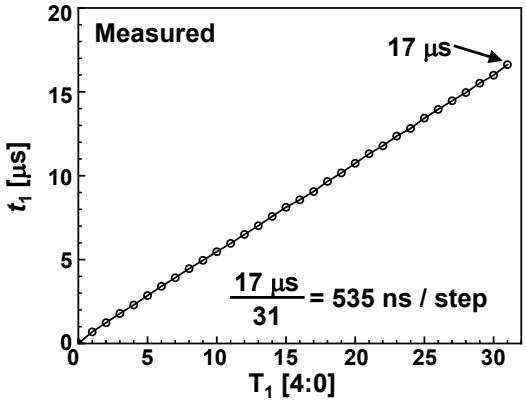

Fig. 7. Measured t_1 vs. T_1 [4:0].

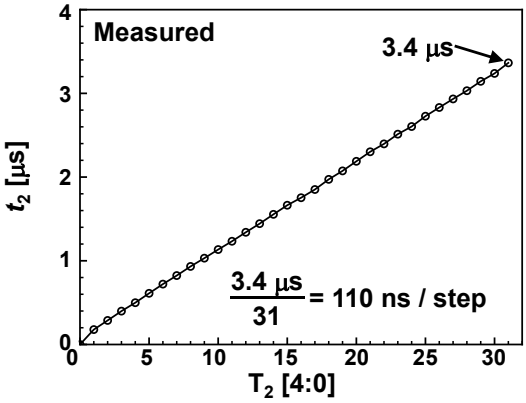

Fig. 8. Measured t_2 vs. T_2 [4:0].

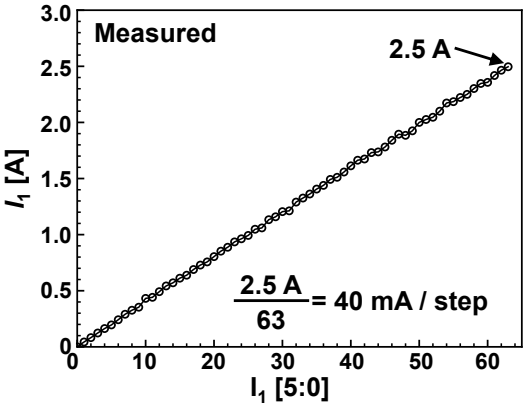

Fig. 9. Measured I_1 vs. I_1 [5:0].

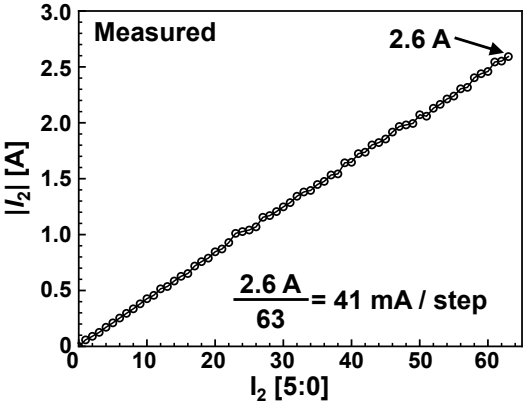

Fig. 10. Measured $|I_2|$ vs. I_2 [5:0].

VDOS means the drop in V_{GS} from 18V that occurs in the t_1 period when I_D exceeds I_{TH}. The advantage of the proposed method is that I_{TH} is variable using VDOS, because the SiC overheating changes by varying Q_C using T_2 [4:0] and/or I_2 [5:0].

C. *Reasons for "V_{GS} Drop due to Overheating of SiC (VDOS)"*

The reasons for VDOS is explained below. In Fig. 6, during t_2, the on-resistance of the SiC MOSFET increases, when V_{GS} is lowered by discharging Q_C. As a result, V_{DS} increases and the SiC MOSFET generates more heat, because the power determined by $V_{DS} \times I_D$ is consumed. When the SiC MOSFET junction temperature (T_J) exceeds a certain value, the gate leakage ($I_{G,LEAK}$) of the SiC MOSFET begins to flow and V_{GS} drops during t_1.

Fig. 11 shows an equivalent circuit that illustrates the principle of VDOS during t_1. R_{ON} is the on-resistance of the gate driver, $R_{G,INT}$ is the internal gate resistance of the SiC MOSFET, and $R_{G,LEAK}$ is the resistance of the gate dielectric of the SiC MOSFETs due to $I_{G,LEAK}$. Fig. 11 shows that $R_{G,LEAK}$ is a function of T_J. As T_J increases, $I_{G,LEAK}$ increases and $R_{G,LEAK}$ decreases, and thus V_{GS} decreases due to resistance divider, which is the reasons for VDOS. I_{TH} can be controlled by Q_C. For example, increasing Q_C lowers I_{TH}, because it increases the V_{GS} drop, V_{DS}, heat generation, and T_J increase.

The physics of $I_{G,LEAK}$ in SiC MOSFETs is explained below. Unlike silicon power devices, SiC MOSFETs are known to have $I_{G,LEAK}$ during a short circuit [16-22]. This $I_{G,LEAK}$ was first reported in 2015 in [16], and in [17] it was reported that $I_{G,LEAK}$ flows during a short circuit in all five commercially available SiC MOSFETs.

The following three stages of phenomena occur in SiC MOSFETs during a short circuit as T_J increases.

- Stage 1: High power due to short-circuit current under high voltage (e.g. 300 V × 300 A = 90 kW) causes T_J of SiC MOSFETs to increase in the order of microseconds. For example, [20] shows that T_J rises from room temperature to 800 °C in 2.7 μs.
- Stage 2: When T_J reaches about 800 °C [20], thermally excited electrons overcome the SiC-SiO_2 interface barrier and $I_{G,LEAK}$ begins to flow [18, 19, 21], as shown in the band diagram in Fig. 12 (a). This phenomenon is called Schottky emission [18, 19, 21]. The SiC MOSFETs are not yet broken, because Schottky emission is an electrothermal phenomenon [18, 21].
- Stage 3: When T_J reaches about 1100 °C [20], the SiC MOSFETs are destroyed due to thermomechanical reasons [21].

The proposed overcurrent protection method in this paper is a technique to detect and protect SiC MOSFETs from overcurrent in Stage 2, before they are destroyed.

Note that $I_{G,LEAK}$ due to Schottky emission in Stage 2 does not occur in silicon power devices [18], because the barrier height at the Si/SiO_2 interface (3.2 eV) is higher than that at the SiC/SiO_2 interface (2.7 eV), as shown in the band diagram in Fig. 12, and thus T_J at which Schottky emission occurs is higher than the thermal runaway temperature of silicon [18].

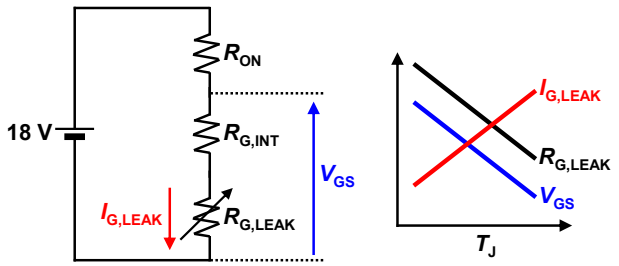

Fig. 11. Equivalent circuit that illustrates principle of VDOS during t_1.

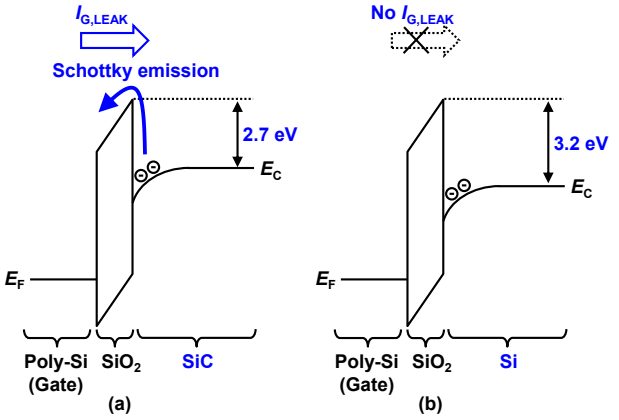

Fig. 12. Band diagram of n-type MOSFET in strong inversion. (a) SiC MOSFET. (b) Si MOSFET.

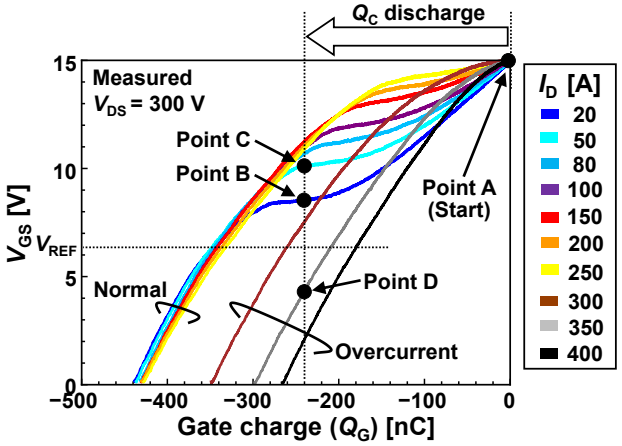

Fig. 13. Measured V_{GS} vs. gate charge of SiC module (BSM120D12P2C005).

III. Measured Results

A. *Gate-Charge Curve to Understand MGDC*

To quantitatively understand the principle of MGDC operation in case of no VDOS, Fig. 13 shows the measured gate-charge curve (V_{GS} vs. gate charge (Q_G)) of the SiC module used in this paper (BSM120D12P2C005, 1200 V rating) with a DC rating of 134 A and a pulse rating of 240 A at V_{DS} = 300 V. Since MGDC repeats Q_C discharge and charge from the initial state of SiC MOSFET turned on, unlike the typical gate-charge curve, Q_G at V_{GS} = 15V is defined as zero.

As an example, the operation of MGDC at Q_C = 240 nC is described below. In case of I_D = 20A, when Q_C is discharged, the operating point moves from Point A with V_{GS} = 15 V to Point B with V_{GS} = 8 V. In case of I_D = 50A, when Q_C is discharged, the operating point moves from Point A with V_{GS} = 15 V to Point C with V_{GS} = 10 V. Furthermore, at I_D = 350 A, which exceeds the pulse rating of 240 A for this SiC MOSFET, when Q_C is discharged, the operating point moves from Point A with V_{GS} = 15 V to Point D with V_{GS} = 4 V.

Therefore, when the SiC MOSFETs operate in the normal region, the Miller plateau voltage increases with increasing I_D, increasing V_{GS} after Q_C discharge, in contrast, when the SiC MOSFETs operate in the overcurrent region, the gate capacitance decreases with increasing I_D, decreasing V_{GS} after Q_C discharge. Since V_{GS} in normal and overcurrent regions are different, the overcurrent can be detected by comparing V_{GS} and V_{REF} using a comparator.

B. Overcurrent Protection with Variable I_{TH}

Figs. 14 and 15 show a circuit schematic and a photo of the measurement setup for a single-pulse test of an inductive load of 34 µH at 300 V for the SiC module (BSM120D12P2C005), respectively.

Fig. 16 shows the conventional measured waveforms of the overcurrent exceeding 350 A. In the conventional desaturation detection, the overcurrent is detected by the V_{DS} increase in Fig. 16. In Fig. 16, the SiC MOSFET is turned off manually. VDOS does not occur in Fig. 16, because V_{GS} is constant at 18 V after turn-on and no heating during t_2 period of MGDC occurs.

Figs. 17 (a) to (f) show the measured waveforms of the proposed overcurrent protection with variable I_{TH} from 306 A to 104 A by changing Q_C. t_1 = 1.9 µs, t_2 = 0.52 µs, and I_1 = 1.6 A are fixed, and Q_C (= $|I_2| \times t_2$) is changed by varying only $|I_2|$ to change I_{TH}. In Figs. 17 (a) to (f), $|I_2|$ is varied from 0.53 A to 0.74 A by varying I_2 [5:0] by one from 13 to 18, respectively, and Q_C is varied from 276 nC to 385 nC, where $|I_2| = I_2$ [5:0] × 41 mA. Increasing Q_C accelerates SiC MOSFET heating and increases VDOS, which lowers I_{TH}. In Fig. 17, "(1) Q_C discharge in t_2, (2) comparison of V_{GS} and V_{REF} at the end of t_2, and (3) recharge to V_{GS} = 18 V in t_1", is repeated in $t_1 + t_2$ cycles. When $V_{GS} < V_{REF}$, overcurrent is detected, Alarm changes from low to high, Internal_ONOFF changes from high to low, and the gate driver is forced to turn off to complete the overcurrent protection. The overcurrent protection delay in Fig. 17 (a) is 207 ns. By changing Q_C from 276 nC to 385 nC, I_{TH} is reduced from 306 A to 104 A, because increasing $|I_2|$ increases V_{DS} during t_2, which increases VDOS due to the increased overheating of SiC. In contrast, in IGBTs, the Q_C dependence of I_{TH} is very small and I_{TH} is almost constant, since VDOS does not occur [13].

Figs. 18 (a) to (d) show the Q_C dependence of I_{TH}, V_{REF}, the overcurrent protection delay, and the relative loss increase due to MGDC (RLI) extracted from Fig. 17, respectively. The definition of RLI is as follows

$$\mathrm{RLI} = \frac{\left(\int_{t_{START}}^{t_{END}} I_D V_{DS} dt\right)_{\text{With MGDC}} - \left(\int_{t_{START}}^{t_{END}} I_D V_{DS} dt\right)_{\text{Without MGDC}}}{\left(\int_{t_{START}}^{t_{END}} I_D V_{DS} dt\right)_{\text{Without MGDC}}} \times 100$$

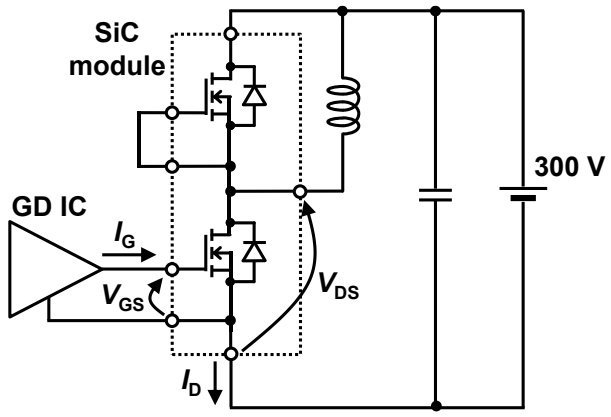

Fig. 14. Circuit schematic of single-pulse test with inductive load.

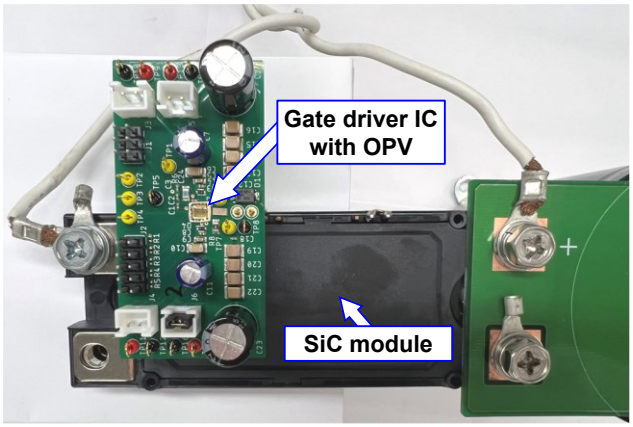

Fig. 15. Photo of measurement setup.

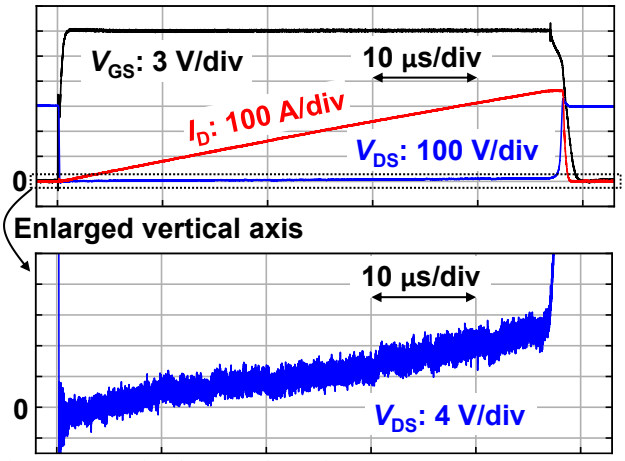

Fig. 16. Conventional measured waveforms.

where t_{START} and t_{END} indicate the start and end time of the single-pulse test, respectively.

As shown in Fig. 18 (a), increasing Q_C from 276 nC to 385 nC enables I_{TH} to be varied from 306 A to 104 A. Since the SiC MOSFET used in this paper has a DC rating of 134 A and a pulse rating of 240 A, the users of the gate driver can freely set I_{TH} in a wide range from 134 A or lower to 240 A or higher, which is a major advantage of this proposal.

As shown in Fig. 18 (b), the proposed overcurrent protection does not work unless V_{REF} is manually adjusted to the

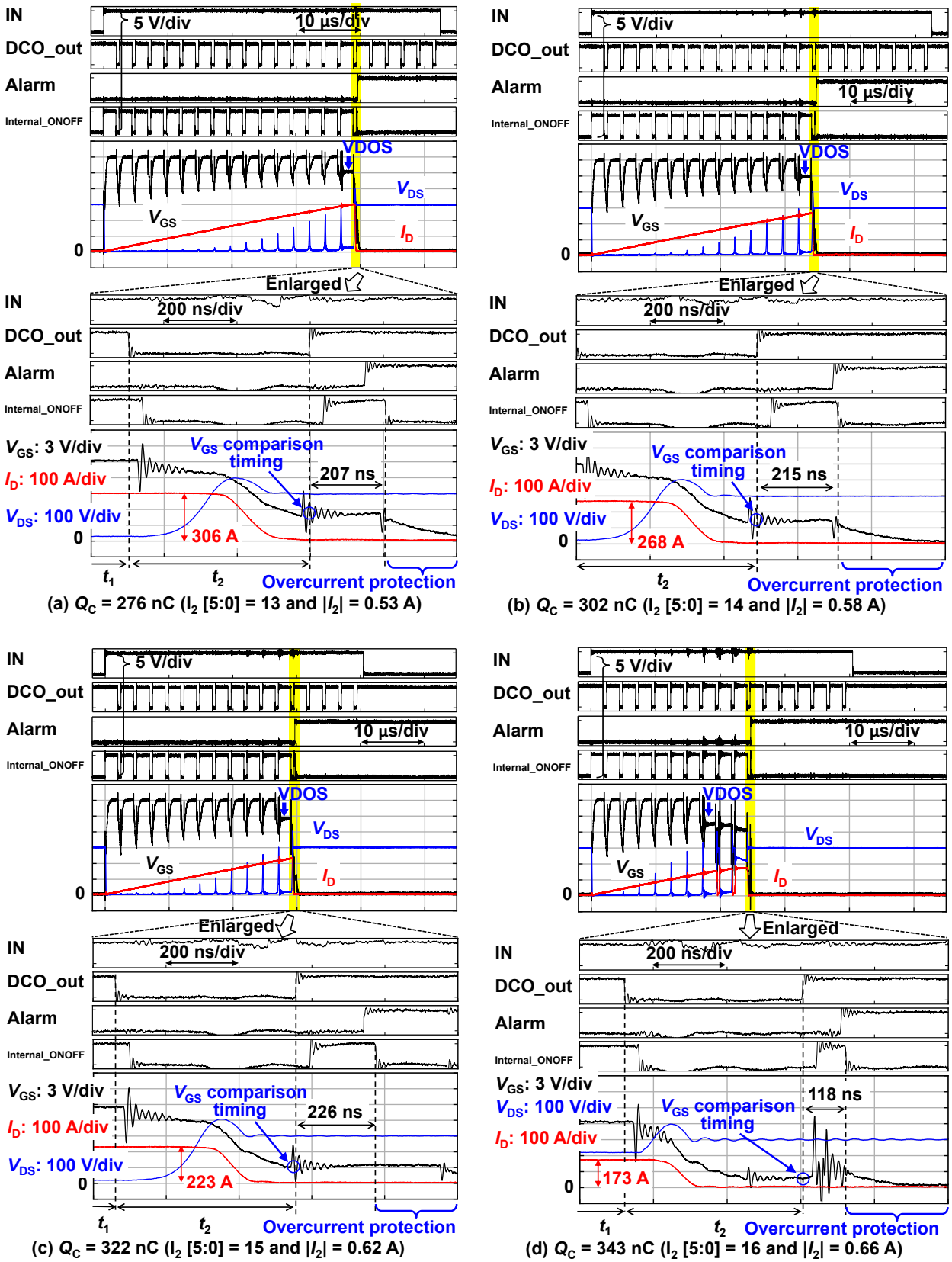

Fig. 17 (a) to (d). Measured waveforms of proposed overcurrent protection with variable I_{TH} from 306 A to 104 A by changing Q_C. (a) Q_C = 276 nC (I_2 [5:0] = 13 and $|I_2|$ = 0.53 A). (b) Q_C = 302 nC (I_2 [5:0] = 14 and $|I_2|$ = 0.58 A). (c) Q_C = 322 nC (I_2 [5:0] = 15 and $|I_2|$ = 0.62 A). (d) Q_C = 343 nC (I_2 [5:0] = 16 and $|I_2|$ = 0.66 A).

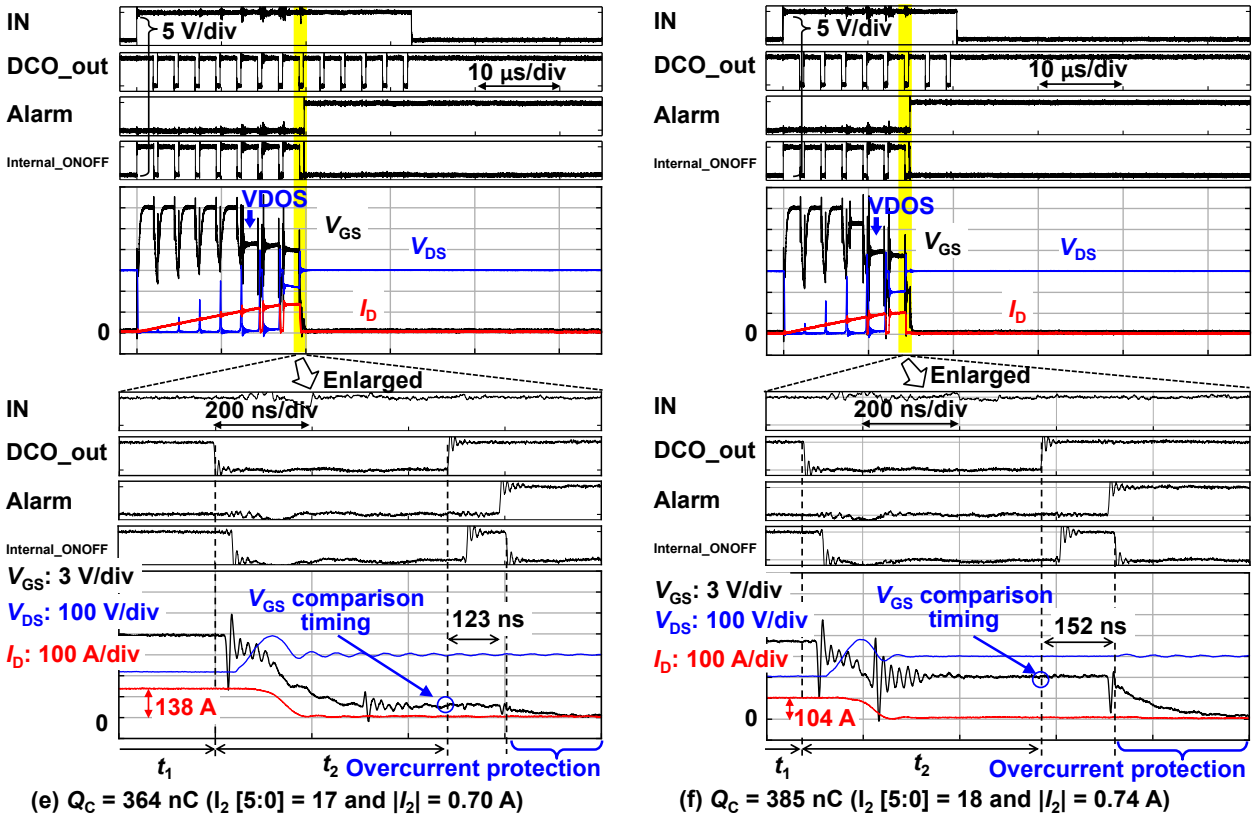

Fig. 17 (e) to (f). Measured waveforms of proposed overcurrent protection with variable I_{TH} from 306 A to 104 A by changing Q_C. (e) Q_C = 364 nC (I_2 [5:0] = 17 and $|I_2|$ = 0.70 A). (f) Q_C = 385 nC (I_2 [5:0] = 18 and $|I_2|$ = 0.74 A).

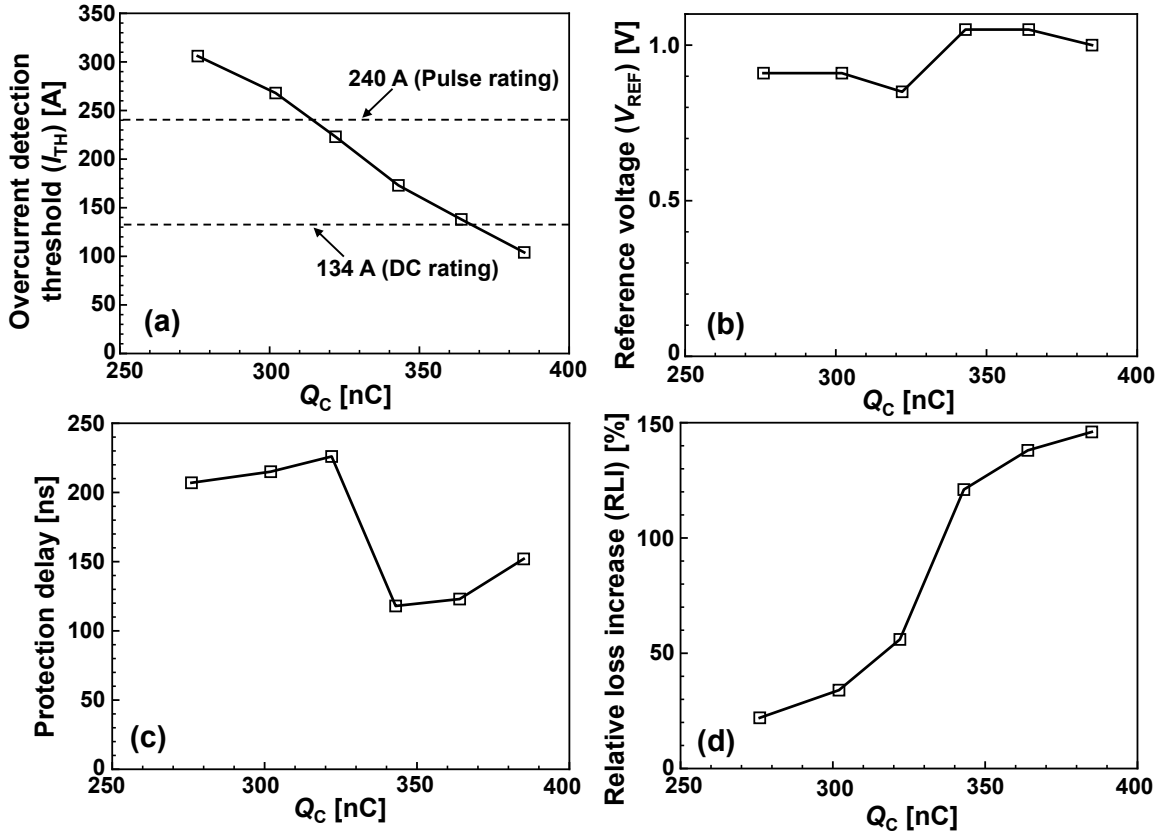

Fig. 18. Q_C dependence extracted from Fig. 17. (a) I_{TH}. (b) V_{REF}. (c) Overcurrent protection delay. (d) Relative loss increase due to MGDC (RLI).

appropriate value depending on Q_C. From the viewpoint of practicality, V_{REF} should be fixed or automatically adjusted, thus the method of setting V_{REF} is a future challenge in this proposal.

As shown in Fig. 18 (c), depending on Q_C, the overcurrent protection delay varies in the range of 118 ns to 226 ns, because the difference between V_{GS} and V_{REF} at the V_{GS} comparison timing (specifically the rise edge of DCO_out) in Fig. 6 is not constant, and the comparator delay varies.

As shown in Fig. 18 (d), increasing Q_C from 276 nC to 385 nC increases RLI from 22% to 146%. Increasing Q_C increases RLI, which is also true for IGBTs [13]. It is inevitable that the Q_C discharge will increase RLI, because the proposed overcurrent protection method detects the overcurrent by monitoring the change in V_{GS} caused by the Q_C discharge. Reducing RLI by optimizing the MGDC parameters is a future challenge in this proposal. For MGDC in IGBTs, RLI has been successfully reduced to 0.8% by parameter optimization [13].

Table I shows a comparison table of detection and protection for overcurrent. This paper is the first work achieving the fully integrated overcurrent protection method for SiC MOSFETs while the SiC MOSFETs are ON with variable I_{TH}.

IV. Conclusions

The overcurrent protection method with variable I_{TH} and fully integrated in the gate driver IC is proposed, which can detect overcurrent while SiC MOSFETs are ON. In the overcurrent protection measurements of the SiC MOSFET with the DC rating of 134 A and the pulse rating of 240 A, by changing Q_C from 276 nC to 385 nC, I_{TH} is reduced from 306 A to 104 A, the overcurrent protection delay varies in the range of 118 ns to 226 ns, and RLI increases from 22% to 146%. The variable I_{TH} is a major advantage of this proposal.

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